partitioning the complete clock net into a global clock net and a plurality of local clock nets, simulating a load for each of the local clock nets, simulating the global clock net, and combining the simulations to form a complete clock net simulation. The method may further include evaluating the combination to determine whether the results converge and storing the simulation results in a Clock Data Model. When the results do not converge, the method re-simulates at least one of the local clock nets and re-simulates the global clock net. The Clock Data Model collects, manages, retrieves, and queries all of the simulation information. The method may further analyze the complete clock net to predict the clock skew for a given data transfer path for potential redesign.--

Please amend the paragraph beginning at line 4 on page 11 as follows:

--Turning now to FIG. 6, a logic flow diagram of a method of determining clock insertion delays for a microprocessor design having grid-based clock distribution is shown. The method uses as an input a database containing the entire network information for the microprocessor. This includes the complete clock net information. Typically, the method extracts each piece of information from this database only once but this may not necessarily be the case. The process begins at START. At block 30, the process partitions the complete clock net into a global clock net and a plurality of local clock nets. The global clock net includes levels ten through three and those portions of level two that are outside of all of the plurality of local clock nets. Each of the plurality of local clock nets includes portions of level two and level one. The location of the local clock nets can be determined in any of a number of ways. One valid approach is to break the complete clock net into a plurality of parts approximating rectangular grid coordinates. The designation of the global clock net may be thought of as horizontal partitioning. The designation of local clock nets may be thought of as vertical partitioning. It may be desired or required to

break one or more of the local clock nets down even further. This would result in sub-, sub-sub-, etc. local clock nets. At block 32, the process simulates each of the plurality of local clock nets. The process will be described in more detail below. If sub-local clock nets were created in block 30, then the lowest sub-local clock net is simulated first and then each successively higher sub-local clock net is simulated until the highest local clock net has been simulated. In those instances when the simulations of the local clock nets do not depend on one another, they may be processed in parallel. The result is a load for each of the local clock nets on the global clock net. This load may take many forms. One valid form is that of a single capacitor for each of the connections of the local clock net to the global clock net. At block 34, the process simulates the global clock net based in part on the simulated load of each of the plurality of local clock nets. This will also be described in more detail below. At block 36, the process combines the simulations to form a complete clock net simulation. At decision block 37, the complete clock net is evaluated to determine if the results converge. It is possible, if somewhat unlikely, that this block could be eliminated. Often, the results of the first pass will not converge as one would prefer and blocks 32 through 37 will be repeated at least once if not more. More details of this iteration aspect of the method will be described below.--

Please amend the paragraph beginning at line 8 on page 14 as follows:

--Returning to FIG. 6, taken together, blocks 32-36 and the blocks of FIGS. 7 and 8 result in the initial set up of the CDM. Recall that in FIG. 7 each of the plurality of local clock nets was simulated under the assumption that the clock arrival times from the global clock net would be simultaneous at all points where the local clock net is connected to the global clock net. Recall further that these times were subsequently calculated in block 34 and FIG. 8. As a result, the assumed clock arrival value and the actual clock arrival value can be compared in block 37.